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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/815,448	04/01/2004	Soon-Hong Ahn	8021-227 (SS-19246-US)	7782

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EXAMINER	
LE, THAO X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 09/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/815,448	AHN ET AL.	
	Examiner	Art Unit	
	Thao X. Le	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-24 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over US 5576557 to Ker et al.

Regarding claim 1, Ker discloses a semiconductor device in fig. 2 comprising: a first well 23 connected to a pad 2, fig. 2, to which an external pin is connected, the first well 23 including a first-type diffusion region N+ (with Rw3) that receives a well bias voltage (Vdd), a second well (p-substrate to the left and right of well 22) adjacent to the first well 23, a second well including an insulating region 22 and at least one second-type diffusion region P+ (with Vss or Rsub1) outside the insulating region 22, fig. 2; and a third well 21 adjacent to the second well and including a first-type diffusion region N+ (with Rw1) that receives a first voltage (Vdd), fig. 2, wherein the insulating region 22 inside the second well having a first-type diffusion region N+ (with Rw2) along with the first-type diffusion N+ (with Rw3) region of the first well 23 constitute a bipolar junction transistor which operates in a cut-off mode and cuts off current flowing from the first well 23 to the third well 21.

The recitation of 'which operates in a cut-off and cuts off current flowing from the first well to the third well.' is only a statement of the inherent properties of the product. The structure recited in the Ker's reference is substantially identical to that of the claims, claimed properties or functions are presumed to be inherent. Or where the claimed and prior art products are identical or substantially identical in structure or composition, or are produced by identical or substantially identical processes, a *prima facie* case of either anticipation or obviousness has been established. *In re Best*, 195 USPQ 430, 433 (CCPA 1977) and MPEP 2112.01.

With respect to second well, the substrate is a P-type substrate, i.e. lightly dope; thus substrate would be interpreted as a well, see also Chiang (6514785) in col. 3 line 10, Cheng (6972463) in col. 3 line 9, or Lojek (6998670) in col. 4 line 11.

Regarding claim 2, Ker discloses the semiconductor device, wherein the at least one second-type diffusion region P+ (with Vss or Rsub1) outside the insulating region 22 comprises a first second-type diffusion region P+ (with Vss or Rsub1) and a second second-type diffusion region 26, and the second well comprises: a first sub-well (P-substrate left of N-well 22) arranged between the insulating region 22 and the first well 23 and including the first second-type diffusion region P+; and a second sub-well (p-substrate right of N-well 22) arranged between the insulating region 22 and the third well 21 and including the second second-type diffusion region P+ 26, wherein the

insulating region 22 is a third sub-well 22 having a first-type diffusion region N+ (with Rw2).

Regarding claim 3, Kerr discloses the semiconductor device wherein the first and second sub-wells (left and right P-substrate portions of N-well 22) of the second well are P-wells (p-substrate), and the first voltage Vss is applied to the second-type diffusion regions P+ of the first and second sub-wells of the second well, fig. 2.

Regarding claim 4, Kerr discloses the semiconductor device wherein the third sub-well 22 is an N-well, fig. 2, and a second voltage is applied to the first-type diffusion N+ region of the third sub-well, fig. 2.

Regarding claim 5, Kerr discloses the semiconductor device wherein the first voltage is a ground voltage, and the second voltage generates a backward voltage between a base and an emitter of a bipolar junction transistor, the bipolar junction transistor comprising the first-type diffusion region N+ of the first well, the second-type diffusion region P+ of the first sub-well, and the first-type diffusion region N+ of the third sub-well.

Regarding claim 6, Kerr discloses the semiconductor device wherein the first 23 and third wells 21 are N-wells, fig. 2b.

Regarding claim 7, Kerr discloses the semiconductor device wherein the well bias voltage applied to the first-type diffusion region N+ of the first well is a power supply voltage, fig. 2

Regarding claim 8, Ker discloses the semiconductor device wherein a region to which the pad 2 is connected is a second-type diffusion region P+ 27, fig. 2.

Regarding claim 9, Kerr discloses the semiconductor device wherein the first-type diffusion regions are formed of N-type impurities, and the at least one second-type diffusion region is formed of P-type impurities, fig. 2

Regarding claim 10, Kerr discloses the semiconductor device wherein the insulating region 22 of the second well has a structure that surrounds the first well 23 fig. 2.

Regarding claims 11, 18, Kerr discloses the semiconductor device wherein the third well 21 constitutes a depletion-type MOS transistor.

Ker discloses a structure recited in the reference is substantially identical to that of the claims, claimed properties or functions are presumed to be inherent. Or where the claimed and prior art products are identical or substantially identical in structure or composition, or are produced by identical or substantially identical processes, a *prima facie* case of either anticipation or obviousness has been established. *In re Best*, 195 USPQ 430, 433 (CCPA 1977) and MPEP 2112.01.

Regarding claim 12, Kerr discloses a semiconductor device in fig. 2 comprising: a first N-well 23 connected to a pad 2 to which an external pin is connected, the first N-well 23 including an N-type diffusion region N+ that receives a well bias voltage (Vdd), and a P-type diffusion region 27, formed in the vicinity of the pad 2; a first P-well (p-substrate to the left and right of N-well 22) adjacent to the first N-well 23, the first P-well including an insulating region 22 and at least one P-type diffusion region P+ (with Rsub1) that receives a ground voltage (Vss) outside the insulating region 22; and a second N-well 21 adjacent to the first P-well and including an N-type diffusion region

N+ (with Rw1) that receives the ground voltage (Vdd), wherein the insulating region 22 is a sub-N-Well 22 embedded with said first P-well and having an N-type diffusion region N+ (with Rw2) that receives an off mode control voltage for preventing a latch-up current, fig. 3.

With respect to 'that receives an off mode control voltage for preventing a latch-up current', Ker discloses a structure recited in the reference is substantially identical to that of the claims, claimed properties or functions are presumed to be inherent. Or where the claimed and prior art products are identical or substantially identical in structure or composition, or are produced by identical or substantially identical processes, a *prima facie* case of either anticipation or obviousness has been established. *In re Best*, 195 USPQ 430, 433 (CCPA 1977) and MPEP 2112.01.

Regarding claim 13, Kerr discloses the semiconductor device wherein the at least one P-type diffusion region P+ comprises a first P-type diffusion region P+ (with Rsub1) and a second P-type diffusion region 26, fig. 2, and the first P-well comprises: a first sub-P-well (left P-substrate of N-well 22) located between the insulating region 22 and the first N-well 23 and including the first P-type diffusion region P+ (with Rsub1); and a second sub-P-well (right P-substrate of N-well 22) located between the insulating region 22 and the second N-well 21 and including the second P-type diffusion region P+ 26, fig. 2..

Regarding claim 14, Kerr discloses the semiconductor device wherein the N-type diffusion region N+ (with Rw3) of the first N-well 23, the P-type diffusion region of the

first sub-P-well, and the N-type diffusion region (with Rw2) of the insulating region 22 constitute a bipolar junction transistor which cuts off a current flowing from the first N-well to the second N-well.

The recitation of 'cuts off current flowing from the first well to the third well.' is only a statement of the inherent properties of the product. The structure recited in the Ker's reference is substantially identical to that of the claims, claimed properties or functions are presumed to be inherent. Or where the claimed and prior art products are identical or substantially identical in structure or composition, or are produced by identical or substantially identical processes, a *prima facie* case of either anticipation or obviousness has been established. *In re Best*, 195 USPQ 430, 433 (CCPA 1977) and MPEP 2112.01.

Regarding claim 15, Kerr discloses the semiconductor device wherein the control voltage generates a backward voltage between a base and an emitter of the bipolar junction transistor composed of the N-type diffusion region of the first N-well, the P-type diffusion region of the first sub-P-well, and the N-type diffusion region of the insulating region.

With respect to 'a backward voltage between a base and an emitter of the bipolar junction transistor', the structure recited in the Ker's reference is substantially identical to that of the claims, claimed properties or functions are presumed to be inherent. Or where the claimed and prior art products are identical or substantially identical in structure or composition, or are produced by identical or substantially identical processes, a *prima facie* case of either

anticipation or obviousness has been established. *In re Best*, 195 USPQ 430, 433 (CCPA 1977) and MPEP 2112.01.

Regarding claim 16, Kerr discloses the semiconductor device wherein the well bias voltage applied to the N-type diffusion region of the first N-well is a power supply voltage, fig. 2.

Regarding claim 17, Kerr discloses the semiconductor device wherein the insulating region 22 of the first P-well has a structure that surrounds the first N-well, fig. 2.

Regarding claim 19, Kerr discloses a method of forming a semiconductor device comprising: forming a first well 23 connected to a pad 2, fig. 2, to which an external pin is connected, the first well 23 including a first-type diffusion region N+ (with Rw3) that receives a well bias voltage (Vdd); forming a second well (second well comprises P-substrate in both side of N-well 22) adjacent to the first well 23, the second well including an insulating region 22 and at least one second-type diffusion region P+ (with Rsub1) outside the insulating region 22; and forming a third well 21 adjacent to the second well and including a first-type diffusion region N+ (with Rw1) that receives a first voltage (Vdd), wherein the insulating region 22 inside the second well having a first-type diffusion region N+ (with Rw2) along with the first-type diffusion region N+ of the first well constitute a bipolar junction transistor, fig. 3b, which cuts off current flowing from the first well to the third well.

The recitation of 'cuts off current flowing from the first well to the third well.' is only a statement of the inherent properties of the product. The structure

recited in the Kerr's reference is substantially identical to that of the claims, claimed properties or functions are presumed to be inherent. Or where the claimed and prior art products are identical or substantially identical in structure or composition, or are produced by identical or substantially identical processes, a *prima facie* case of either anticipation or obviousness has been established. *In re Best*, 195 USPQ 430, 433 (CCPA 1977) and MPEP 2112.01.

Regarding claims 20, 22, Kerr discloses the method wherein the at least one second-type diffusion region P+ (with Rsub1) outside the insulating region comprises a first second-type diffusion region P+ (with Psub1) and a second second-type diffusion region P+ 26, and the step of forming a second well comprises: forming a first sub-well (P-substrate to the left of 22) between the insulating region 22 and the first well 23, the first sub-well including the first second-type diffusion region P+ (with Rsub1); and forming a second sub-well (P-substrate to right of 22) between the insulating region 22 and the third well 21, the second sub-well including the second second-type diffusion region P+ 26, wherein the insulating region 22 having a first-type diffusion region N+(with Rw2), wherein the insulating region is a third sub N-well 22.

Regarding claim 21, Kerr discloses the method wherein the first and second sub-wells of the second well are P-wells (P-substrate), and the first voltage is applied to the second-type diffusion regions of the first and second sub-wells of the second well, fig. 2.

Regarding claim 23, Kerr discloses the method wherein the first and third wells 23/21 are N-wells, fig. 2.

Regarding claim 24, Kerr discloses the method wherein the first-type diffusion regions N+ are formed of N-type impurities, and the at least one second-type diffusion region P+ is formed of P-type impurities, fig. 2.

Response to Arguments

3. Applicant's arguments filed 8/25/06 have been fully considered but they are not persuasive.

a. The Applicant argues that Ker does not disclose the N+ region with Rw3 and N+ region with Rw2 constitute a BJP. This is not persuasive because as in fig. 1 and 2 Ker discloses the bipolar junction transistor Q2 and Q3 would be equivalent to D1 and D2, col. 4 lines 63-65 and col. 4 lines 25-26, respectively.

b. With respect to "operate s in a cut-off mode and cut off current from flowing from first well to a third well" or "that receives an off mode control voltage for preventing a latch0up current", the Examiner submits Ker's device has substantially identical structure; thus it would inherently have such function or capable of performing such function. *In re Best*, 195 USPQ 430, 433 (CCPA 1977) and MPEP 2112.01. Furthermore the claims direct to apparatus or device must be distinguished from the prior art in terms of structure rather than function. In re Ludtke, 441 F.2d 660, 169 USPQ 563 (CCPA 1971); and the Applicant fails to show that Ker did not posses the functional characteristics of the claim, Northam Warren Corp. v. D.F. Newfield Co., 7 F. Supp 773, 22 USPQ 313 (E.D.N.Y. 1934) or MPEP 2114.

c. With respect to insulating region, the Examiner submits that N-well 22 with N+ region is equivalent to the "so called" insulating region BR or SW3 or N-well of the instant application.

d. With respect to P-well vs. P-well, the examiner's interpretation is consistent with the art because the P-substrate or P-well is being regarded as the same element that is lightly doped. Such interpretation is substantiated by Chiang (6514785) in col. 3 line 10, Cheng (6972463) in col. 3 line 9, or Lojek (6998670) in col. 4 line 11.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X. Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Sept. 2006

THAO X. LE
PRIMARY PATENT EXAMINER